Overview

ASE Material
- Operation began in July 1995

Vision
- To be the best semiconductor packaging material (Lead Frame & BGA substrate) manufacturer in the world

Products
- Buildup FC substrate
- BGA series substrate
- Etched Lead Frames

Plant floor
- Kaohsiung: 29,000 m²
- Chung Li: 94,000 m² (under re-installation)
- Shanghai: 84,500 m² (Ready)

Manpower
- Kaohsiung, Taiwan: 1,400
- Chung-Li, Taiwan: 100
- Shanghai, China: 1,700 (2,300 in Q4/05)
Development Milestones

1995  Started Etched Leadframe Production
1998  Started BGA/LBGA/TFBGA substrate Production
1999  ISO-9002 Certified
2000  ISO-14001 Certified
2002  QS-9000 Certified
2002  Started GPP (Gold Pattern Plating) Production
2003  Started Flip-Chip Build Up substrate Production
2003  TS 16949 Certified
2004  ASES ISO-9002 Certified
2005  Transfer 450 technical persons from CL to SH.
Worldwide PBGA Substrate Supply
2004 Market Share

- JCI/TCI: 17%
- Nanya: 11%
- Kinsus: 11%
- Samsung: 8%
- PPT: 19%
- ASE: 22%
- Others: 12%

Total Value: $630 million
Total Units: 1,150 million

Source: Prismark Feb. 2005
Plant Location 1

Address: 73, Kai-Fa Road, Nantze Export Processing Zone, Kaohsiung, Taiwan, ROC
Close to Kaohsiung International Airport (30 minutes to drive)
Plant Location 2

A-building destroyed in a fire incidence on 2005/05/01
Recovery in B-Building, will start running in Nov. 2005

Address: 550, Chung-Hwa Rd Section 1,
Chung-Li, Taiwan, ROC
Close to Hsin-Chu Science Park (1Hour) and
CKS International Airport (30 minutes to drive)
Plant Location 3

ASE Shanghai

Address: 599 Li Shi Zhen Rd, Zhang Jiang Hi-Tech Park, Pudong New Area, Shanghai 201203, P.R.C.
Close to Pu Dong International Airport (30 minutes to drive)
Business Area:

Organic substrate and etched leadframe for IC packaging and module assembly.

Product Offerings:

a. 1, 2, 4 & 6 layers substrate for BOC/BGA/CSP/Modules
b. Up to 4+N+4 buildup flip chip substrate
c. High Density Interconnection solution with laser via and fine pitch capability
d. High electrical performance solution with buildup and stubless solution
Laminate Expansion Plan

Unit: M Pcs/Month

50% 2L and 50% 4L, equivalent to 27x27mm.
Substrate Technology & Product introduction
Introduction

- Illustration of Flip Chip Packages

- Die
- Solder Bump
- Underfill
- Substrate
- Solder Ball
Introduction-Cross section of PBGA

- Cap Thickness
- Substrate Thickness
- Overall Thickness
- ball diameter
- Ball pitch
- ball height
PBGA Process Flow(I)

- **Wafer Grinding**
  - **Wafer Mount**
  - **Wafer Saw**
    - 2nd Optical Gate
  - **Die Attach**
  - **Epoxy Cure**
    - Plasma Clean
  - **Wire Bond**
    - 3rd Optical Gate

Diagram:
- **Wafer**
  - **Substrate**
  - **Die (chip)**
  - Conductive epoxy
  - Substrate
  - Gold Wire
PBGA Process Flow (II)

- Plasma Clean II
- Molding
- Post Mold Care
- Marking
- Ball Mount
- Singulation
- Scan & Final Visual
- Packing

Raw Substrate  
After Die Attached  
After Molding  
After Ball Attached
# ASE Package Offerings in Sweet-spot 4C Products

<table>
<thead>
<tr>
<th>Sector</th>
<th>Conventional</th>
<th>Advanced Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Wire Bond</td>
<td>WLP</td>
</tr>
<tr>
<td>Auto/Car</td>
<td></td>
<td></td>
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<tr>
<td>Telemetries</td>
<td>Controller</td>
<td></td>
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<tr>
<td></td>
<td>PA/Passive</td>
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<td></td>
<td>PLD/ASIC</td>
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<td></td>
<td>MAC + BB</td>
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<tr>
<td></td>
<td>BT &amp; WLAN</td>
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<tr>
<td>Comms</td>
<td>Graphic Chip</td>
<td></td>
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<tr>
<td></td>
<td>CPU</td>
<td></td>
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<tr>
<td></td>
<td>Chipset</td>
<td></td>
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<tr>
<td>Computing</td>
<td>Memory Chip</td>
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<td></td>
<td>Controller/</td>
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<td></td>
<td>MPU</td>
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<tr>
<td>Consumers</td>
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<td>Home theater</td>
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</tbody>
</table>

- **Conventional** includes Wire Bond processes.
- **Advanced Package** includes WLP and Flip Chip technologies.
- **SiP** represents System-in-Package solutions.

*Images depict examples of package offerings for each category.*
IC Shipments By Package Category

Source: Prismark 2004
## ASE Packaging Technologies

**Keep Pace With IC Miniaturization**

<table>
<thead>
<tr>
<th>IC Feature Size (nm)</th>
<th>0.13</th>
<th>0.09</th>
<th>0.065</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Packaging</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pitch (µm)</td>
<td>250</td>
<td>200</td>
<td>150</td>
</tr>
<tr>
<td>F/C</td>
<td>45</td>
<td>40</td>
<td>35</td>
</tr>
<tr>
<td>W/B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Substrate</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L/S (µm/µm)</td>
<td>30+/30+</td>
<td>25/25</td>
<td>20+/20+</td>
</tr>
<tr>
<td><strong>Layer Count</strong></td>
<td>2</td>
<td>6</td>
<td>8+</td>
</tr>
<tr>
<td><strong>Green Technology</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pb-Free</td>
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<tr>
<td>Halogen-Free</td>
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<td></td>
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</tr>
</tbody>
</table>
ASE BU Substrate Technology Ahead of Industry

ITRS*

ASE Capability

* 2003 ITRS Roadmap
One-Stop Shopping @ ASE

Module, Board Assembly & Test (DMS)

Final Test

IC Assembly

Wafer Bumping/Probing

Substrates

ASEmtl KH CL SH

Circuit Design

Foundry

Engineering Test

IMC

IBM

Motorola

Qualcomm

USI
Product introduction
<table>
<thead>
<tr>
<th>Market Requirement</th>
<th>Substrate Technology Solution</th>
</tr>
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<tbody>
<tr>
<td><strong>Product</strong></td>
<td></td>
</tr>
<tr>
<td>Flip Chip substrate</td>
<td>Build up 4+N+4</td>
</tr>
<tr>
<td>RF/PA</td>
<td>E/P R,L,C</td>
</tr>
<tr>
<td>Cavity Down BGA</td>
<td>Normal</td>
</tr>
<tr>
<td>PBGA/LFBGA</td>
<td>Build up</td>
</tr>
<tr>
<td><strong>Material</strong></td>
<td></td>
</tr>
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<td>Green Material</td>
<td>BT/NX,E679FG</td>
</tr>
<tr>
<td>AUS308</td>
<td></td>
</tr>
<tr>
<td><strong>Design / New process</strong></td>
<td></td>
</tr>
<tr>
<td>High Density</td>
<td>Pattern Plating</td>
</tr>
<tr>
<td>Fine Pitch</td>
<td>SAP</td>
</tr>
<tr>
<td>OSP</td>
<td>Etch Back</td>
</tr>
<tr>
<td>Electroless Ni/Au</td>
<td>GPP/Selective gold</td>
</tr>
<tr>
<td>Electrical Ni/Au</td>
<td></td>
</tr>
<tr>
<td>Metal finish</td>
<td>Pre-Solder</td>
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Small size – Smaller IC footprint, reduced height and weight.

Improved performance – Short interconnect delivers low inductance, resistance and capacitance, small electrical delays, good high frequency characteristics.

Increased functionality – The use of flip chips allow an increase in the number of I/O. An area array pad layout enables more signal, power and ground connections in less space.
PBGA substrate provides the interconnection platform with the circuit board for assembly package. It could protect and support the ICs with thermal enhancement.
Cavity-down BGA enhance thermal performance by about 15~20% when compared to 4-layer PBGA and by 35% when compared to the 2-layer PBGA.
Spec.

A. Preprint Thickness 5+/-2um.

B. Dielectric 1 16.5+/-3.5um.

C. Middle Electrode 5+/-2um.

D. Dielectric 2 16.5+/-3.5um.

E. Top Electrode 5+/-2um.
### Technology Deployment

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</tr>
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FC Substrate Process Flow (2+2+2)

- **Inner Layer** [3rd & 4th Layers]
- **1st Build-up** [2nd & 5th Layers]
- **2nd Build-up** [1st & 6th Layers]
- **SR create** [Solder Resist]
- **Backend** [Pre-solder / SOP]
**Issue of Material**
Utilize the vertical baking method to release the mechanical stress and increase the panel dimension.

**Thin Cu Etching I**
Reduce the thickness of copper by etching line.

**Mechanical Drilling**
Create connecting channels between mental layers by using mechanical drilling machine.

**Plating Through Hole (PTH)**
Enabling hole wall to connect conducting metal between layers.
[sub-process: Desmear, E’less Cu & Cu Plating]
**Plugging Pretreatment**
Roughening the copper surface in order to increase the adhesions between ink fluid and hole wall.

**Ink Plugging**
Fulfill the PTH vacancy to avoid the shape distortion, collapsing and oxidation. [sub-process: plugging and baking]

**Grinding I**
Grind off the protrusion of ink fluid by non-woven buff.

**Thin Cu Etching II**
Reduce the thickness of copper by etching line.

**Grinding II**
Grind off the protrusion of ink fluid by non-woven buff again.
Lid Plating
Enhance the reliability of the substrate by adding copper cap, also it is designed for the stagger via and stacked via on PTH structure. [sub-process: Desmear, E‘less Cu & Cu Plating]

Etch Resist Lamination
Treat laminate with some pre-treating chemical to make the copper surface ready for resist coating. [sub-process: pretreatment and lamination]

Lid Plating
Enhance the reliability of the substrate by adding copper cap, also it is designed for the stagger via and stacked via on PTH structure. [sub-process: Desmear, E‘less Cu & Cu Plating]

Exposure
Using plotted artwork film and UV exposure machine to transfer the pattern image from artwork to boards.

Developing
The pattern shape resist will form first after developing, leaving copper to be removed exposed on non-exposure areas.

Pattern Etching
Acid chemistry used to etch the copper in areas where the photoresist has been developed. Removal of base copper from the innerlayer.
1st Build-up [2rd & 5th layers]

**Lamination Pretreatment**
Cleaning and roughening the copper surface used by acid/alkaline chemistry agent for vacuum lamination preparation.

**Vacuum Lamination**
The application of ABF to a printed circuit pattern through the use of heat, pressure and time [sub-process: lamination and baking]

**Laser Drilling**
Drill microvias barrel on the ABF surface by the Laser radiation drilling technique to create connecting channels inbetween the dielectric with copper area.

**Desmear**
The removal of smeared epoxy-resin from copper surfaces within the microvia barrel to facilitate a connection with plated copper.
**Electro-less Cu**
The chemistry used to deposit copper onto the flat areas and inside the drilled holes often outlayer panel.

**Dry-film Lamination**
The process of covering a circuit pattern with a thin layer of dry film photoresist. [sub-process: pretreatment and lamination]

**Exposure**
Using plotted artwork film and UV exposure machine to transfer the pattern image from artwork to boards.
Developing
The process in which the unpolymerized phoeresist is removed from the copper surface.

Dry-film Stripping
Strip off all of the etching resist remaining (ie. dry film) and leave the copper circuit pattern only.

Etching
Removal of base copper through the etching line.

Electrolytic Cu Plating
The copper and tin plating method using an electrical current.
2nd Build-up [1st & 6th layers]

**Lamination Pretreatment**
Cleaning and roughening the copper surface used by acid/alkaline chemistry agent for vacuum lamination preparation.

**Vacuum Lamination**
The application of ABF to a printed circuit pattern through the use of heat, pressure and time. [sub-process: lamination and baking]

**Laser Drilling**
Drill microvias barrel on the ABF surface by the Laser radiation drilling technique to create connecting channels inbetween the dielectric with copper area.

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The chemistry used to deposit copper onto the flat areas and inside the drilled holes often outlayer panel.

Dry-film Lamination
The process of covering a circuit pattern with a thin layer of dry film photoresist. [sub-process: pretreatment and lamination]

Exposure
Using plotted artwork film and UV exposure machine to transfer the pattern image from artwork to boards.

Developing
The process in which the unpolymerized photoresist is removed from the copper surface.
**Electrolytic Cu Plating**
The copper and tin plating method using an electrical current.

**Dry-film Stripping**
Strip off all of the etching resist remaining (ie. dry film) and leave the copper circuit pattern only.

**Etching**
Removal of base copper through the etching line.
Solder Mask Printing
A polymeric non-conductive coating applied to the surface of a circuit board to protect the circuit traces and laminate surface.

Exposure
Using plotted artwork film [ie. dry film] and UV exposure machine to transfer the solder mask opening image from artwork to boards.

Developing
Create the openings on solder mask surface.

Post-baking
The final step in the application of solder mask is curing, whether by heat or by ultraviolet light. [sub-process: post-baking, UV curing, Plasma]
Backend

**De-panel**
Cutting a penal into 1/4 multipack.
[sub-process: routing and post-cleaning]

**OSP**
Deposit the organic solderability preservative on the copper surface of solder mask openings in order to prevent oxidation occurring. [sub-process: Preclean, Cu etching, OSP]

**Bump Printing**
Print the eutectic solder bump cream into each solder mask openings.
**Solder Reflow**
Utilize solder reflow chamber with temperature profiles to consolidate the eutectic solder bump cream into solder balls.

**Deflux**
Remove the residues of flux that remained on the solder mask after solder reflow.

**Singulation**
Saw each multi-pack into a single unit.

**Coining**
Create co-planarity of solder bump by the bump coining machine.

**O/S test**
Test the electric current to find whether a circuit trace has a blockage or lose an electrical signal across the entire width of the circuit.
Process: Micro via/Build up

Laser drill and Mechanical drill

30~100um  50~100um

Normal 6 Layer

Build-up(2+2+2)

Plated bump Cu filled via

Adhesive layer

Single step laminating

Stacked via Pad on via

Fine pattern

High Layer Count SSP

14 Layers  X:Y = 1:2.36
Process: Fine pitch – SAP (Semi Additive Process)

Tenting process:
Line/Space = 35um/35um

SAP: Line/Space = 15um/15um
**Process: Stub-less (Etching Back/GPP/SG)**

**Plating Bar**
- Less Design Routable
- Cross-Talk (RF Concern)
- O/S can't be applied

**Etching Back**
- Plating Buss Still Need in Design
- Still Stub Residual
- O/S can be applied

**GPP (Gold Pattern Plating)**
- Really Stubless, Design Routable
- Good Electrical Performance
- O/S can be applied
Process: GPP (Gold Pattern plating) / SG (Selective Gold Process)

Characteristic
1. Stub-less Design (Reduce noise scattering from plating trace)
2. High IO Density
3. High Reliability (Reduce adhesion problem between SM with Au surface)

Etching Back   GPP   Selective Gold
• What is ENIG:

*Electroless Nickel Immersion Gold*

• What is ENAG:

*Electroless Nickel Autocatalytic Gold*

• Advantage:

  (+) No need plating bar.

  (+) Can match the wire bonding requirement.

  (+) Equipment cost is inexpensive.

• Shortcoming:

  (-) Poor solder joint strength. (Sn/Ag/Cu)

  (-) Few suppliers for supporting.

  (-) Difficult control for autocatalytic gold tank.

  (-) Chemical cost is expensive.
Process: Pre-solder

ENIG Ni plating

Pre clean ➔ Cu etching ➔ Pd depositing ➔ Ni depositing
Ni thk: 5 ± 2um

ENIG Au Plating

Au thk: 0.075 ± 0.025um

OSP coating

150um Bump Pitch
OSP: Organic Solderability Preservatives
AFOP substrate: Au on Finger, OSP on Pad.

Structure

Normal PBGA

AFOP Substrate

Normal Substrate

(+ ) Normal process flow
(+ ) Not ball pad oxidation concern
(- ) Poor solder joint strength (SnAgCu)
(- ) Missing ball (SnAgCu)

AFOP Substrate

(+ ) High solder joint strength
(+ ) Longer fatigue life for solder join
(- ) Unable to measure OSP THK
(- ) Tighten control of WIP
Thank you !!

Q&A