# A Wideband 0.18 $\mu$m CMOS LNA with RC-Feedback Topology for UWB Applications

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***Abstract*** **- A 0.18 μm CMOS low noise amplifier using RC-feedback topology is proposed with optimized matching, gain, noise, linearity and area for UWB applications. The IC prototype achieved 9.5 dB of average power gain, low 3.4 dB noise figure (NF), -9.2 dB input match, -13.5 dB return loss, -6 dBm of IIP3 and only 0.54 mm$^2$ size with 15 mW power consumption. Good agreement between the simulated and measured results is found.**

## I. Introduction

The Federal Communications Commission (FCC) has distributed 7500 MHz bandwidth for ultra-wideband (UWB) applications. Ultra-wideband technology using the unlicensed frequency band from 3.1 to 10.6 GHz has become much interest of broadband wireless communication due to its high data rates, low power transmission, robustness for multi-path fading and low power dissipation. Among possible applications, UWB technology may be used for imaging systems, vehicular and ground penetrating radars, and communication systems. For such broadband applications, the low noise amplifier (LNA) is the first stage in the UWB receiver. It must provide good input impedance matching, low power consumption, low noise performance and sufficient gain with good S/N for the following stages, and small size over the entire frequency band [1]-[13]. Recently, the CMOS technology is a candidate for UWB LNA system [7]-[19] when considering the time to market, hardware cost, the degree of difficulty, and high integration with baseband digital circuits – for a good System-on-Chip (SoC) solution. However, these performance requirements for UWB are very challenging using CMOS technology. This is because the CMOS technology can only provide small gain at high frequency, low cut-off frequency ($f_T$) [20]-[22], significant substrate loss [23]-[24] and poor inductor *Q*-factors [22] compared with GaAs technology. Several different circuit approaches, including distributed amplifier (DA), LC ladder, current-reused, shunt feedback, etc., have been proposed to overcome these issues [7]-[19].

The RC-feedback cascode topology is one of the main methods for wideband amplifier design [11]-[16]. The RC-feedback cascode configuration can provide good input matching and improve gain flatness. However, the challenge of this technique is very wide bandwidth along with low noise and high gain. In this work an ultra-wideband CMOS LNA is proposed a cascode amplifier with three stages: new RC-feedback cascode topology, LC shunt configuration and output current buffer technology, implemented in 0.18 μm CMOS technology. With new RC-feedback cascade connection and LC shunt techniques, this LNA achieved a 9.5 dB average power gain, a 3.4 dB NF, input reflect loss less than -9.2 dB, output return loss less than -13.5 dB and the input IIP3 is -6 dBm from ultra-wide band LNA circuit. These results are suitable for UWB LNA circuit application.

## II. Circuit Design

The UWB LNA requires high gain, low noise figure and high linearity over the entire band with low power consumption. The LNA also needs to have a good input mating over the whole band to capture the transmitted RF energy efficiently. Figure 1 shows a schematic of the proposed three stages amplifier. The first stage is the capacitance-resistance feedback cascode topology that provides high gain, wider bandwidth, better stability and well reverse isolation. The middle stage is an inductor-capacitor parallel configuration ($L_B$//$C_B$) to pull up high frequency gain. The output stage is a simple current buffer that gives broadband output impedance of 50 Ω for measurement purposes. This circuit was designed with Agilent's Design System (ADS), and implemented in TSMC's 0.18 μm RF CMOS technology.

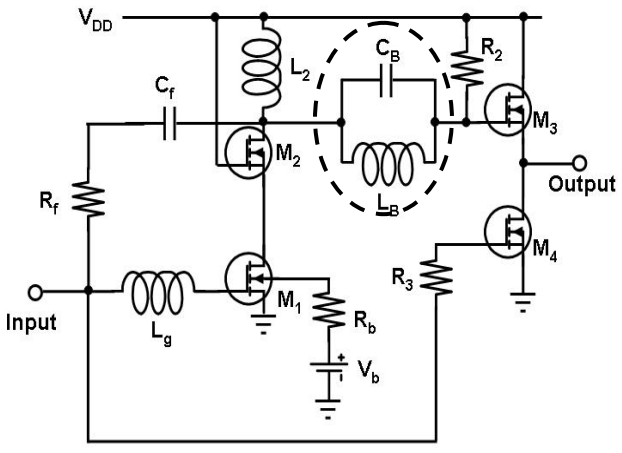


Fig. 1. Schematic of the ADS-designed UWB CMOS RC-feedback LNA circuit. The dashed circle is $L_B$//$C_B$ shunt topology.

For input matching, we used RC-feedback cascode topology for matching. The cascode configuration can reduce the high frequency roll-off of the input devices due to the Miller effect. It provides input and output matching independently. We can select $Z_f$ ($R_f$ and $C_f$ components) to achieve good input matching and high gain. The output stage of the RC-feedback LNA circuit is used current buffer ($M_3$ and $M_4$ transistors) to tune the whole frequency to achieve 50 Ω. The $M_3$ is the source follower and the $M_4$ provide the stable current source for $M_3$. We only fine tune the bias and transistors size to achieve good output matching.

Among several topologies that provide a gain over a wideband, the RC-feedback loop is one of the most popular to use in amplifiers circuit for its wideband input matching and good linearity [11]-[13]. The substrate bias of transistor $M_1$ is used to raise the gain and reduce the power dissipation. However, the gain was confined at high frequency due to gate-drain capacitance and gate-source capacitance. For further rise up the gain at higher frequency, an inductor-capacitor parallel configuration ($L_B$//$C_B$) was connected to the second stages to extend bandwidth as the dashed circle in Fig. 1. The $L_B$//$C_B$ is chosen to resonate at 10.6GHz for the bandwidth extension. The power gain ($S_{21}$) can increase at high frequency. The wide band and high gain was obtained in our LNA circuit design.

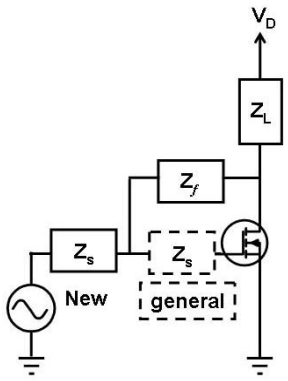


Fig. 2. The schematic of input stage for RC-feedback UWB LNA added noise circuit. The solid line is our work and the dash line is general design for comparison.

The RC-feedback topology in first stage is dominated the noise characteristics for LNA. To analysis the noise performance of the RC-feedback CMOS amplifier, the noise sources are added to the schematic circuit of first stage as shown in Fig. 2, also comparison with general circuit design [12]-[17]. Compare with general circuits, the proposed feedback topology is connected in front of the matching gate inductor ($L_g$). From the noise circuit, the total noise $v_i^2$ of the general design circuit is one item ($i_f^2 R_{Lg}^2$) more than that of our circuit due to the noise current $i_f$ does not go through the $L_g$. The $NF_{min}$ of new FB circuit and general design are compared using ADS simulated as shown in Fig. 3. The NF can be reduced 0.54 dB at high frequency. Therefore, the noise figure can be reduced using new feedback topology circuit. A high voltage and low noise UWB LNA can be achieved. The observation of our design is presented in the following section.

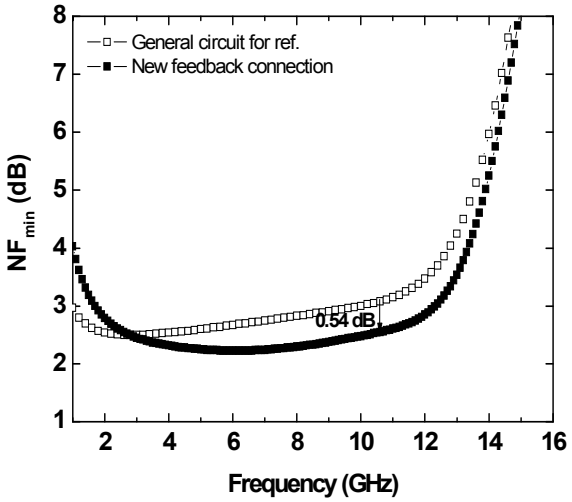


Fig. 3. Simulated noise figure ($NF_{min}$) using new feedback topology and general circuit for comparison.

## III. Results And Discussion

The CMOS UWB LNA was tested via on-wafer probing. A network analyzer and ATN-NP5B noise-parameter system meter were used to measure the small-signal *S*-parameters and *NF* over the frequency range from 1 to 16 GHz. Fabricated in 0.18 μm 1P6M standard CMOS process this prototype chip using power supply of 1.8 V consumes 15 mW including the output buffer stage. The microphotograph of fabricated CMOS UWB LNA with a chip size 0.54 $mm^2$ including the probe pads is shown in Figure 3.

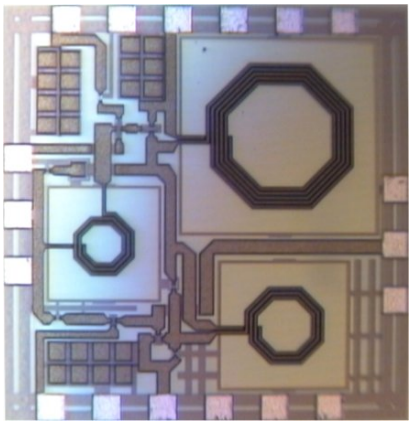

Fig. 3. Image of the fabricated RC-Feedback UWB LNA.

Figures 4 and 5 show the two-port measured S-parameters from 1 GHz to 16 GHz. Figure 4 shows the dependence of measured input reflection coefficient ($S_{11}$) and output return loss ($S_{22}$) on frequency. The measured $S_{11}$ was lower than -9.2 dB for input matching across the frequency band of 3.1~10.6 GHz. The measured $S_{22}$ was less than -13.5 dB for output matching over a 3.1~10.6 GHz range. In Figure 5 the measured forward gains ($S_{21}$) and reverse isolation ($S_{12}$) are reported for

the UWB LNA circuit. The $S_{21}$ displays a maximum gain of 11.7 dB at 3.1 GHz and the average $S_{21}$ value over the 3.1-10.6 GHz frequency band is 9.5 dB. With RC-feedback cascade topology, the bandwidth extends to cover from 3.1 to 10.6 GHz. An excellent $S_{12}$ of less than -25.7 dB was obtained due to effective cascode configuration. It is noted that the input impedance was optimized for low noise figure while keeping the corresponding return loss at an acceptable level.

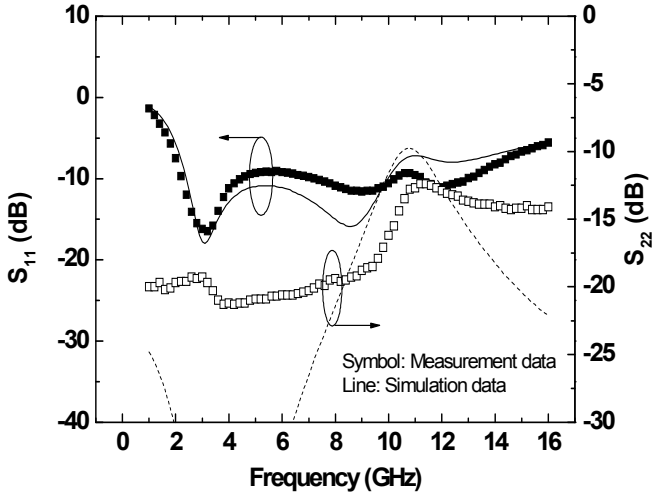


Fig. 4. Measured and simulated input return loss ($S_{11}$) and output loss ($S_{22}$) of the RC-Feedback UWB LNA.

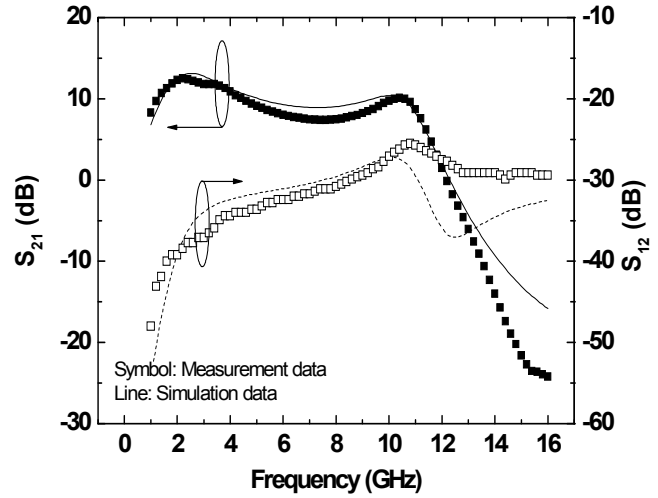


Fig. 5. Measured and simulated power gain ($S_{21}$) and reverse isolation ($S_{12}$) of the RC-Feedback UWB LNA.

To optimize the performance, the transistors have been sized to provide good noise characteristics, while allowing a good input impedance matching over the required bandwidth. The measured NF of the implemented amplifier is shown in Figure 6. The measured NF shows a minimum value of 3.41 dB at 9 GHz. The measured NF range was 3.41~ 4.04 dB over the 3.1~10.6 GHz range. Figure 7 shows the two-tone test for third-order intermodulation distortion of the UWB CMOS LNA circuit. The third order input intercept point (IIP3) is -6 dBm.

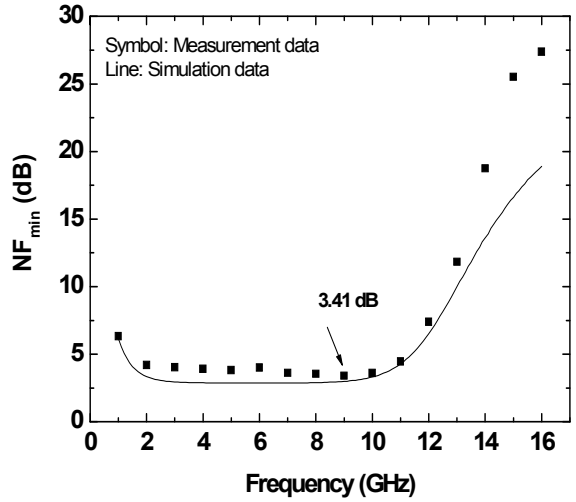


Fig. 6. Measured and simulated noise figure ($NF_{min}$) of the RC-Feedback UWB LNA.

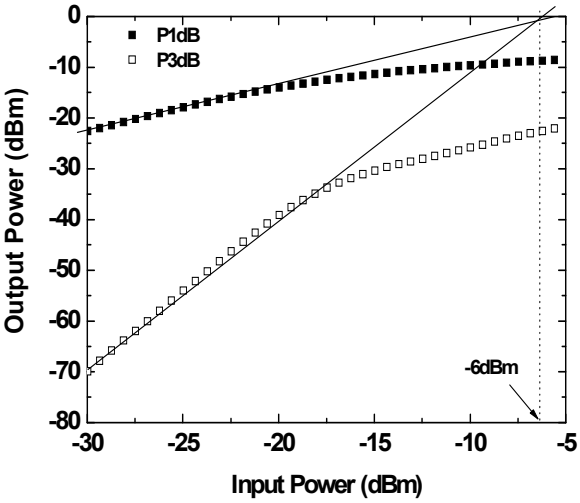


Fig. 7. Measured IIP3 of the RC-Feedback UWB LNA.

Table 1 summarizes the measured performance of the LNA and compares the other reported circuit performance. Our proposed CMOS LNA can achieve a wide bandwidth, high gain, good linearity, low *NF* and low power consumption, and compares well with other published reports [15]-[17].

Table 1. Comparison of LNA circuit performance: published and this work.

| Ref. | [15] | [16] | [17] | This Work |
|---|---|---|---|---|
| BW (GHz) | 2.8 ~ 7.2 | 3.1 ~ 10.6 | 1.2 ~ 11.9 | 3.1 ~ 10.6 |
| $S_{11}$ (dB) | < -4 | <-9.7 | < -11 | < -9.2 |
| $S_{22}$ (dB) | < -7.5 | N/A | N/A | < -13.5 |
| Gain (dB) | 16 ~ 19.5 | 7.4 ~ 9.2 | 5 ~ 9.7 | 7.5 ~ 11.7 |
| $NF_{min}$ (dB) | 3.1 ~3.8 | 4.1 ~ 7 | 4.2 ~ 5.1 | 3.4 ~4.04 |
| IIP3 (dBm) | -1 | 7.25 | -6.2 | -6 |
| PD (mW) | 32 | 23.5 | 20 | 15 |
| Area ($mm^2$) | 1.63 | 0.78 | 0.59 | 0.54 |
| Topology | 0.18 µm Feedback | 0.18 µm Feedback | 0.18 µm Noise-Canceling | 0.18 µm Feedback |

## IV Conclusion

A CMOS UWB LNA with new RC-feedback connection has been designed. This UWB LNA exhibited a high 11.7 dB gain, low 3.4 dB NF, input reflect loss less than -9.2 dB, output return loss less than -13.5 dB and the input IIP3 is -6 dBm from 3.1 to 10.6 GHz, while only 15 mW power dissipation. The fabricated LNA satisfies UWB LNA system requirements.

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